Listing of Claims:

1. (original): A method for automatically calibrating the frequency range of a phase lock loop (PLL), the method comprising:

providing a loop filter for accumulating charge to generate a loop-filter voltage;

providing a voltage controlled oscillator (VCO) having a plurality of frequency ranges, the VCO receiving the loop-filter voltage and generating an output signal having a frequency according to the loop-filter voltage and a currently selected VCO frequency range;

connecting an input of the loop filter to a constant voltage; and

selecting an optimal VCO frequency range by comparing the frequency of a PLL feedback signal for a plurality of the VCO frequency ranges with the frequency of a reference signal, the PLL feedback signal being generated according to the VCO output signal.

2. (original): The method of claim 1, further comprising providing a feedback divider for generating the PLL feedback signal according to the VCO output signal.

3. (original): The method of claim 1, wherein the optimal VCO frequency range comprises either a first VCO frequency range or an adjacent second VCO frequency range such that the frequency of the PLL feedback signal is faster than the frequency of the reference signal for the first VCO frequency range and the frequency of the PLL feedback signal is slower than the frequency of the reference signal for the second VCO frequency range.

4. (original): The method of claim 3, wherein selecting the optimal VCO frequency range further comprises synchronizing the PLL feedback signal with the reference signal.

5. (original): The method of claim 4, wherein the input of the loop filter is connected to a maximum voltage or a minimum voltage and selecting the optimal VCO frequency range further comprises conducting a linear search starting from a lowest or a highest VCO frequency range and proceeding until the optimal VCO frequency range is found.

6. (original): The method of claim 4, wherein the input of the loop filter is connected to a medium voltage and selecting the optimal VCO frequency range further comprises conducting a binary search starting from a middle VCO frequency range and proceeding until the optimal VCO frequency range is found.

7. (original): The method of claim 6, wherein the optimal VCO frequency range comprises the first VCO frequency range when the time duration between the second rising edges of the reference signal and the PLL feedback signal for the first VCO frequency range is shorter than that of the second VCO frequency range, otherwise comprises the second VCO frequency range when the time duration between the second rising edges of the reference signal and the PLL feedback signal for the second VCO frequency range is shorter than that of the first VCO frequency range.

8. (original): The method of claim 4, wherein finding the first VCO frequency range comprises mapping a divide factor of a feedback divider to a predicted first VCO frequency range.

9. – 14. (cancelled)

15. (original): A phase lock loop (PLL) comprising:

a loop filter for accumulating charge to generate a loop-filter voltage;

a VCO having a plurality of frequency ranges, the VCO receiving the loop-filter voltage and generating an output signal having a frequency according to the loop-filter voltage and a currently selected VCO frequency range; and

calibration logic for selecting an optimal VCO frequency range, wherein during PLL calibration, the input of the loop filter is connected to a constant voltage, and the calibration logic searches for an optimal VCO frequency range by comparing the frequency of a PLL feedback signal for a plurality of the VCO frequency ranges with the frequency of a reference signal, the PLL feedback signal being generated according to the VCO output signal.

16. (original): The PLL of claim 15, further comprising a feedback divider for generating the PLL feedback signal according to the VCO output signal.

17. (original): The PLL of claim 16, wherein the calibration logic further comprises a frequency detector receiving the PLL feedback signal and the reference signal, and wherein the optimal VCO frequency range comprises either a first VCO frequency range or an adjacent second VCO frequency range such that the frequency of the PLL feedback signal is faster than the frequency of the reference signal for the first VCO frequency range and the frequency of the PLL feedback signal is slower than the frequency of the reference signal for the second VCO frequency range.

18. (original): The PLL of claim 17, wherein the calibration logic further comprises a loop controller and during PLL calibration, when searching for the optimal VCO frequency range, the loop controller sends a synchronize signal to the feedback divider to synchronize the PLL feedback signal with the reference signal.

19. (original): The PLL of claim 18, wherein the calibration logic further comprises a switch for selectively connecting the input of the loop filter to a maximum voltage or a minimum voltage depending on a control signal from the loop controller, and wherein during PLL calibration, the calibration logic conducts a linear search starting from a lowest VCO frequency range and proceeding until the optimal VCO frequency range is found.

20. (original): The PLL of claim 18, wherein the calibration logic further comprises a switch for selectively connecting the input of the loop filter to a middle voltage, and wherein during PLL calibration, the calibration logic conducts a binary search starting from a middle VCO frequency range and proceeding until the optimal VCO frequency range is found.

21. (original): The PLL of claim 20, wherein the optimal VCO frequency range comprises the first VCO frequency range when the time duration between the second rising edges of the reference signal and the PLL feedback signal for the first VCO frequency range is shorter than that of the second VCO frequency range, otherwise comprises the second VCO frequency range when the time duration between the first rising edges of the reference signal and the PLL feedback signal for the second VCO frequency is shorter than that of the first VCO frequency range.

22. (original): The PLL of claim 18, wherein the calibration logic further comprises:

a storage unit storing a plurality of predicted first VCO frequency ranges indexed by divide factors for the feedback divider;

wherein during PLL calibration, the calibration logic determines the first VCO operating frequency range according to the predicted first VCO frequency range retrieved from the storage unit according to the divide factor of the feedback divider.